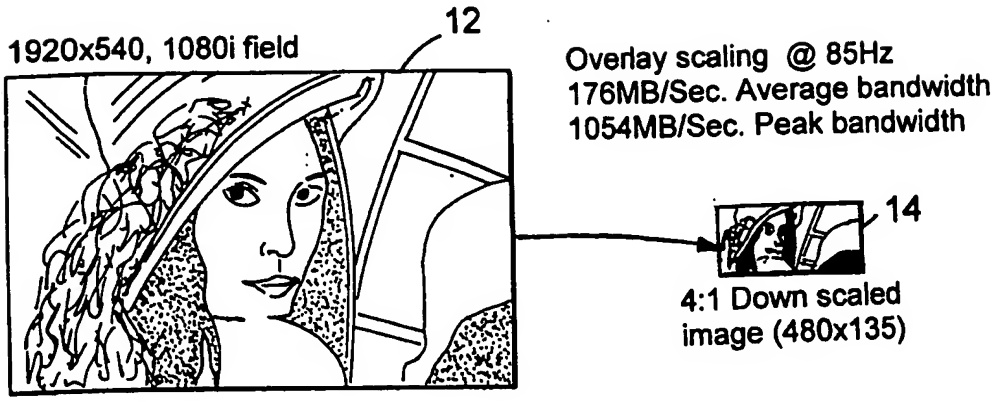

1920x540, 1080i field
12
Overlay scaling @ 85Hz
176MB/Sec. Average bandwidth
1054MB/Sec. Peak bandwidth
14
4:1 Down scaled
image (480x135)

FIG. 1

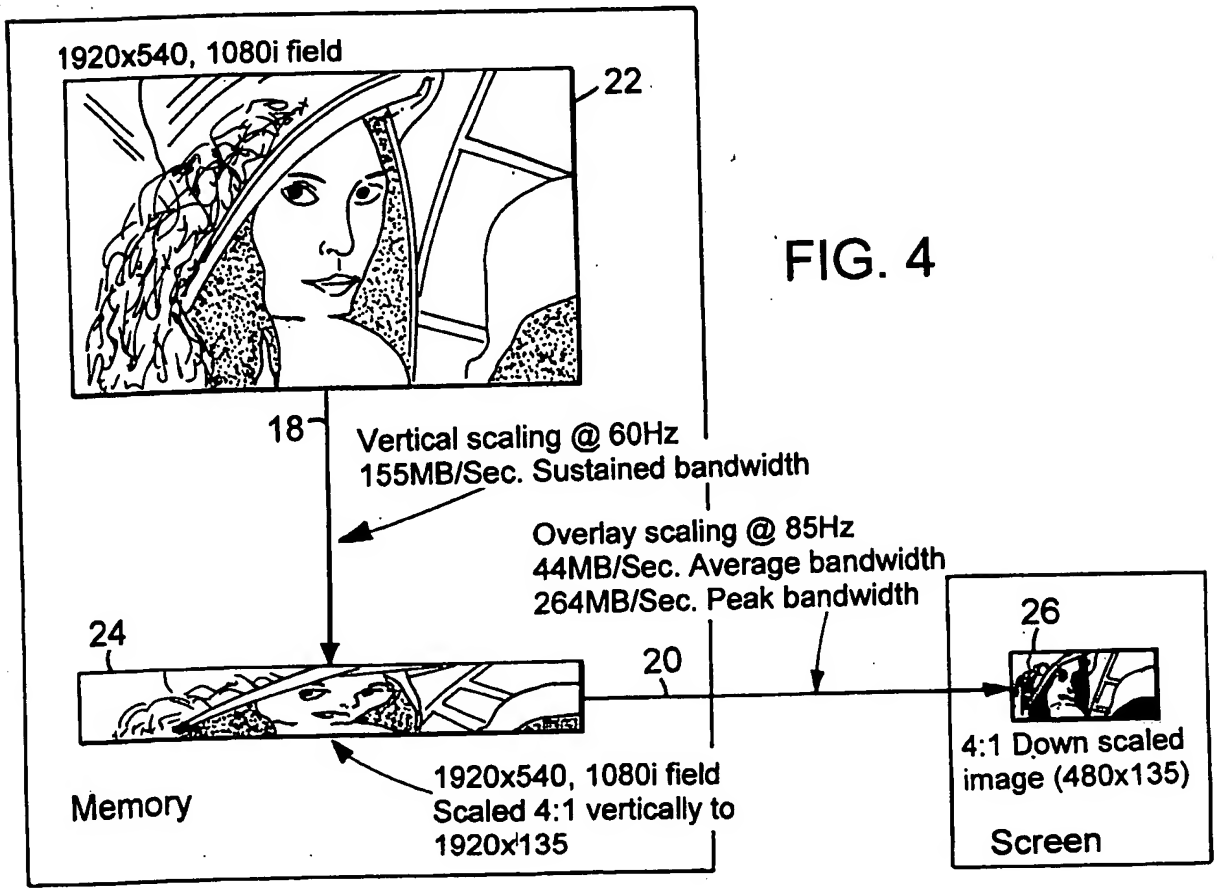

1920x540, 1080i field
22
18
Vertical scaling @ 60Hz
155MB/Sec. Sustained bandwidth
Overlay scaling @ 85Hz
44MB/Sec. Average bandwidth
264MB/Sec. Peak bandwidth
24
20
26
4:1 Down scaled
image (480x135)
Memory
1920x540, 1080i field
Scaled 4:1 vertically to
1920x135
Screen

FIG. 4

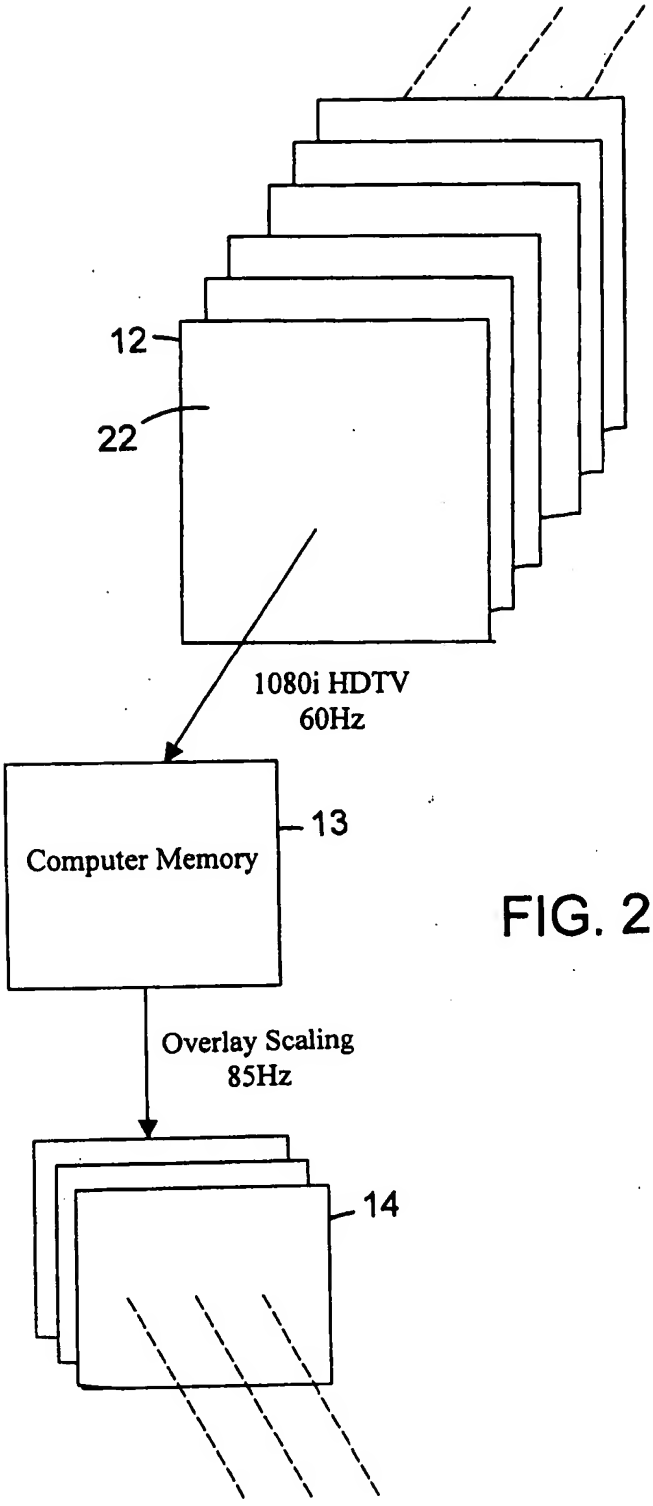
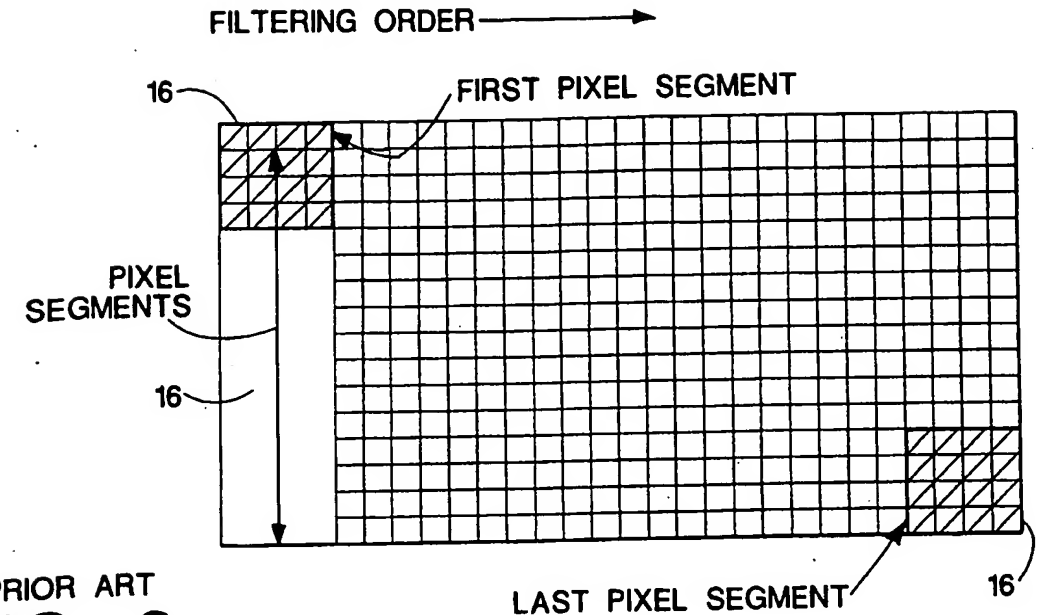

12
22
1080i HDTV
60Hz
Computer Memory
13
Overlay Scaling
85Hz
14

FIG. 2




PRIOR ART
FIG. 3

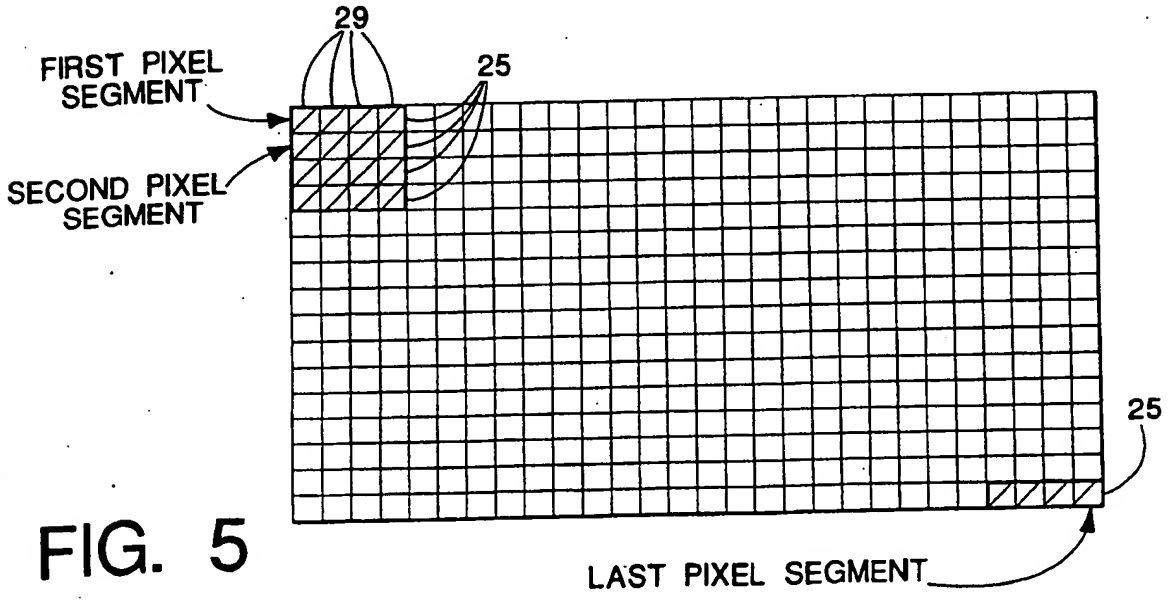



FIG. 5

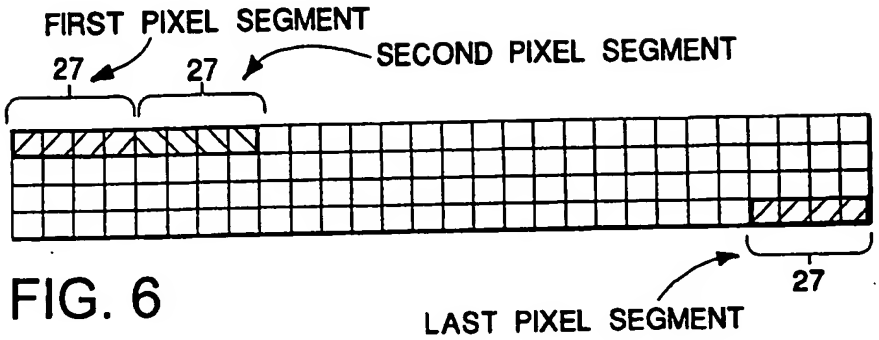



FIG. 6

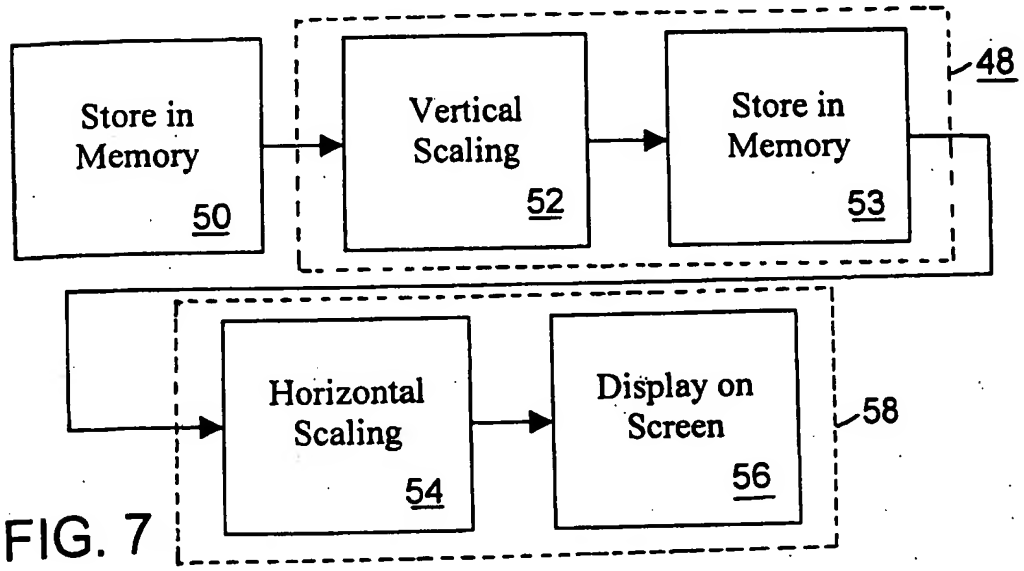



FIG. 7

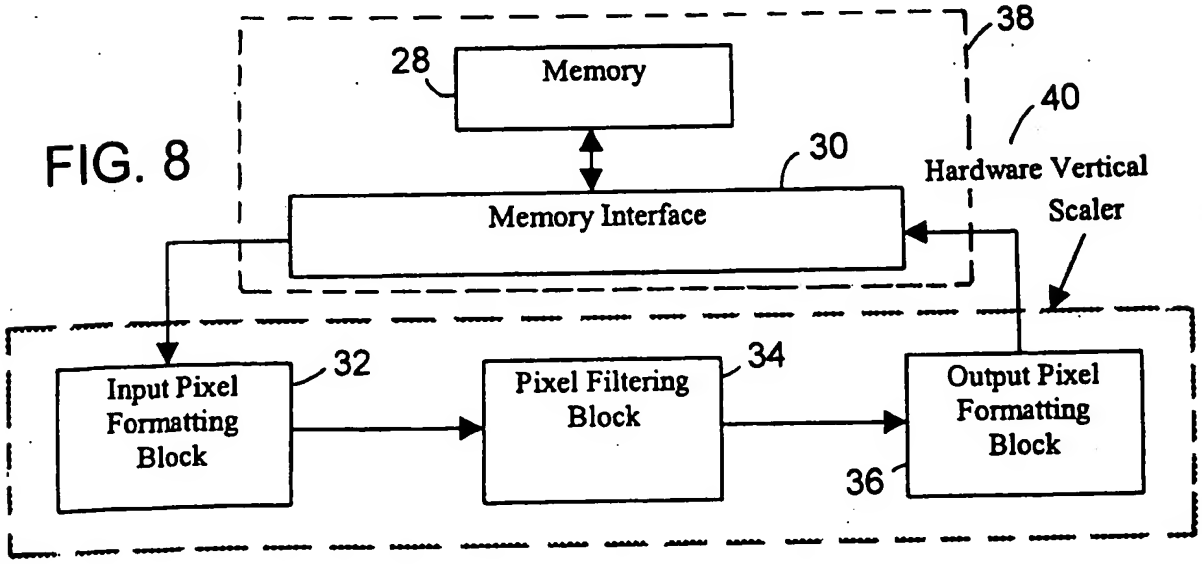



FIG. 8

| | Signal | Description |
|---|---|---|
| | | **Clock and Reset Interface** |
| | HVS_Reset | Hardware Vertical Scaler reset |
| | HVS_Clk | Hardware Vertical Scaler main clock |
| | | **Memory Interface** |
| 78 | Fetch_Ready | Source input image data is available (from Memory Controller) |
| 78 | Fetch_Data[31:0] | Source input image data (from Memory Controller) |
| | | **Register and Command Interface** |
| 60 | Start_Y_Cmnd | Command to start the processing of the Y plane of pixels |
| 66 | Y_Addr[31:3] | Upper 29 bits of the source Y image byte address |
| 68 | Y_Pitch[14:3] | Amount to add to the address to locate the next line's Y pixels |
| 70 | Y_Length[10:0] | Number of lines in the source input Y image plane |
| 72 | Y_Width[11:0] | Number of Y pixels (x4) in one line of the source image |
| 62 | Start_U_Cmnd | Command to start the processing of the U plane of pixels |
| 66 | U_Addr[31:3] | Upper 29 bits of the source U image byte address |
| 68 | U_Pitch[14:3] | Amount to add to the address to locate the next line's U pixels |
| 70 | U_Length[10:0] | Number of lines in the source input U image plane |
| 72 | U_Width[11:0] | Number of U pixels (x4) in one line of the source image |
| 64 | Start_V_Cmnd | Command to start the processing of the V plane of pixels |
| 66 | V_Addr[31:3] | Upper 29 bits of the source V image byte address |
| 68 | V_Pitch[14:3] | Amount to add to the address to locate the next line's V pixels |
| 70 | V_Length[10:0] | Number of lines in the source input V image plane |
| 72 | V_Width[11:0] | Number of V pixels (x4) in one line of the source image |
| | | **Filter Interface** |
| | Filter _Ready | Filter block is ready to accept pixels from the IPFB |

IPFB Input Table

FIG. 9

**Output Table**

| | Signal | Description |
|---|---|---|
| | | **Memory Interface** |
| 78 | Fetch_Req | Request to the memory interface for the source image |
| 78 | Fetch_Addr[31:3] | Upper 29 bits of the source image current byte address |
| | | **Register and Command Interface** |
| 74 | Y_Done | The IPFB has sent the last pixel segment of the Y image to the PFB |
| 74 | U_Done | The IPFB has sent the last pixel segment of the U image to the PFB |
| 74 | V_Done | The IPFB has sent the last pixel segment of the V image to the PFB |
| | | **Filter Interface** |
| 76 | Column_Done | The last pixel of the current column is being sent to the Filter Block |
| | Filter_Req | Request to send the next set of pixels to the Filter Block |
| | Filter _Data[31:0] | The pixel data to the Filter Block |

FIG. 10

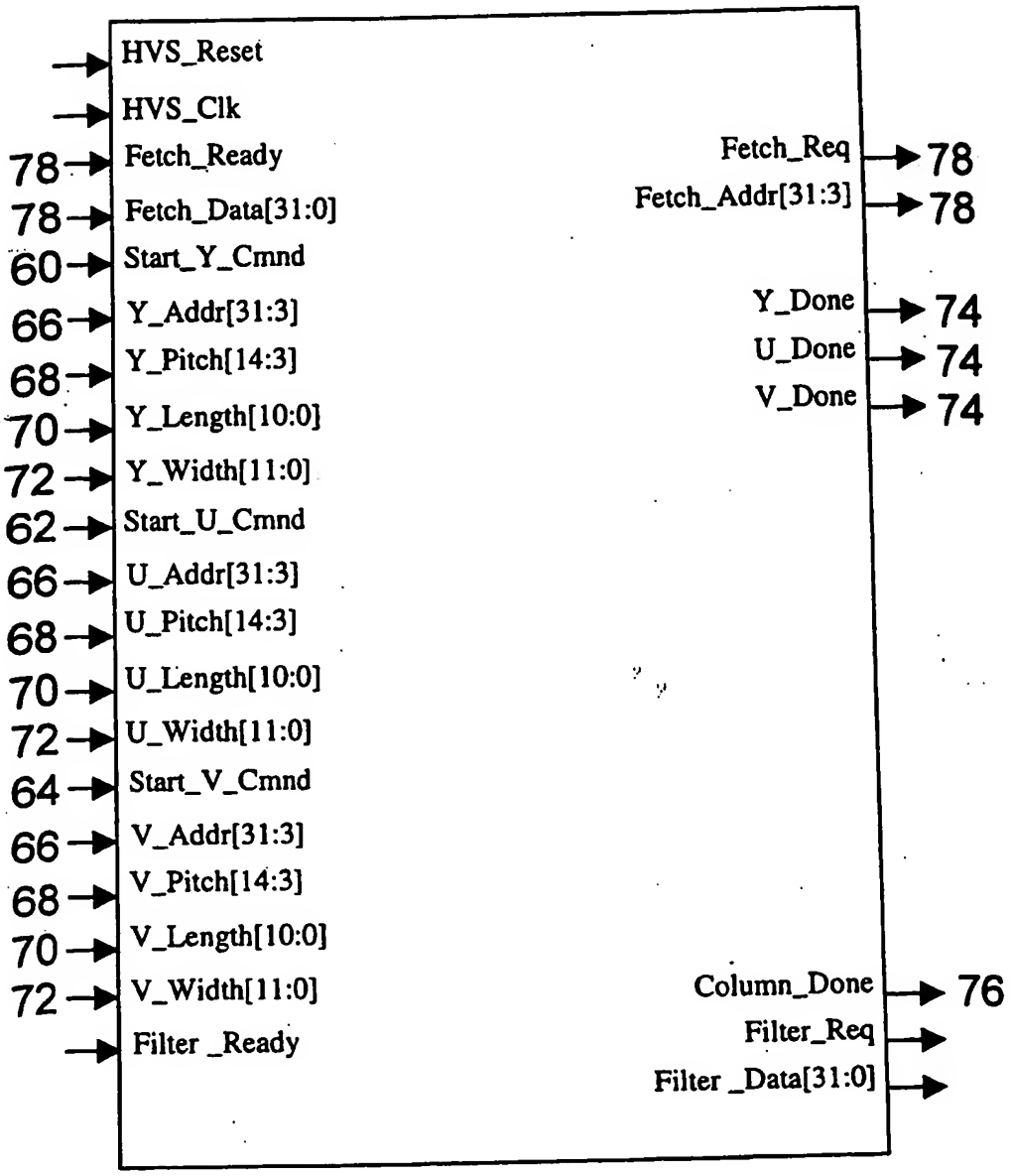

HVS_Reset
HVS_Clk
78
Fetch_Ready
78
Fetch_Data[31:0]
60
Start_Y_Cmnd
66
Y_Addr[31:3]
68
Y_Pitch[14:3]
70
Y_Length[10:0]
72
Y_Width[11:0]
62
Start_U_Cmnd
66
U_Addr[31:3]
68
U_Pitch[14:3]
70
U_Length[10:0]
72
U_Width[11:0]
64
Start_V_Cmnd
66
V_Addr[31:3]
68
V_Pitch[14:3]
70
V_Length[10:0]
72
V_Width[11:0]
Filter _Ready
Fetch_Req
78
Fetch_Addr[31:3]
78
Y_Done
74
U_Done
74
V_Done
74
Column_Done
76
Filter_Req
Filter _Data[31:0]

FIG. 11

**Input Table**

| Signal | Description |
|---|---|
| | **Clock and Reset Interface** |
| HVS_Reset | Hardware Vertical Scaler reset |
| HVS_Clk | Hardware Vertical Scaler main clock |
| | **Input Pixel Formatting Block (IPFB) Interface** |
| Y_Done | The IPFB has sent the last pixel segment of the Y image to the PFB |
| U_Done | The IPFB has sent the last pixel segment of the U image to the PFB |
| V_Done | The IPFB has sent the last pixel segment of the V image to the PFB |
| Column_Done | The last pixel of the current column is being sent to the Filter Block |
| Filter_Req | Request to input the next set of pixels to the Filter Block |
| Filter _Data[31:0] | The pixel data to the Filter Block |
| | **Output Pixel Formatting Block (OPFB) Interface** |
| Scaled_Ready | OPFB is ready to accept pixels from the PFB |
| | **Register and Command Interface** |
| CRAM_Write | Write command to the CRAM port |
| CRAM_Addr[5:0] | CRAM Address for programming coefficients |
| CRAM_Data[6:0] | Seven bit CRAM coefficient data |
| DDA_Write | Write command to the DDA port |
| DDA_Addr[3:0] | DDA Function Address for programming DDA behavior |
| DDA_Data[31:0] | DDA data |

80
82
84

FIG. 12

**Output Table**

| Signal | Description |
|---|---|
| | **Input Pixel Formatting Block (IPFB) Interface** |
| Filter _Ready | Filter block is ready to accept pixels from the IPFB |
| | **Output Pixel Formatting Block (OPFB) Interface** |
| Scaled_Req | Request to transfer data from PFB to OPFB |
| Scaled_Data[31:0] | Scaled output image data from Pixel Filter Block |

FIG. 13

**Pixel Filtering Block (PFB)**

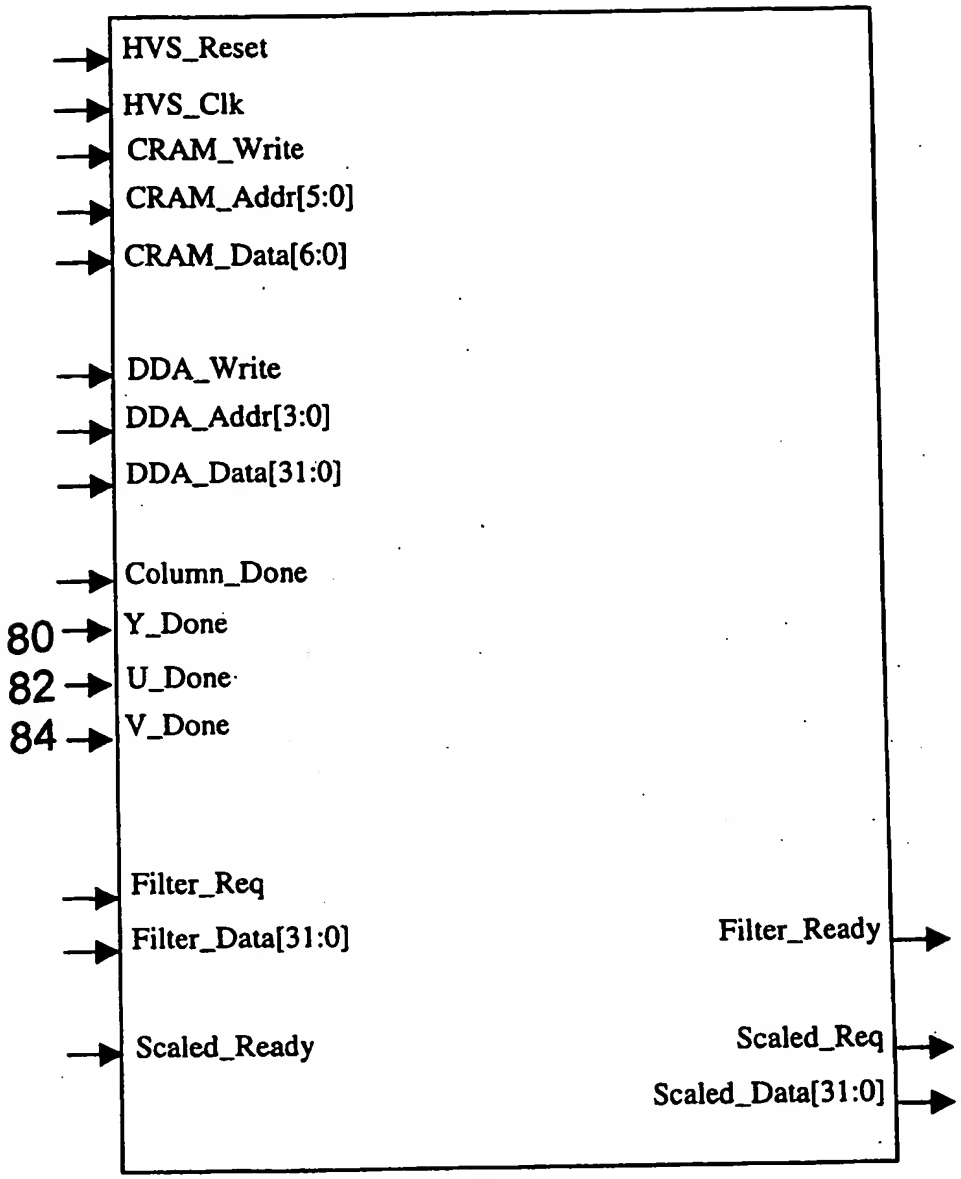



FIG. 14

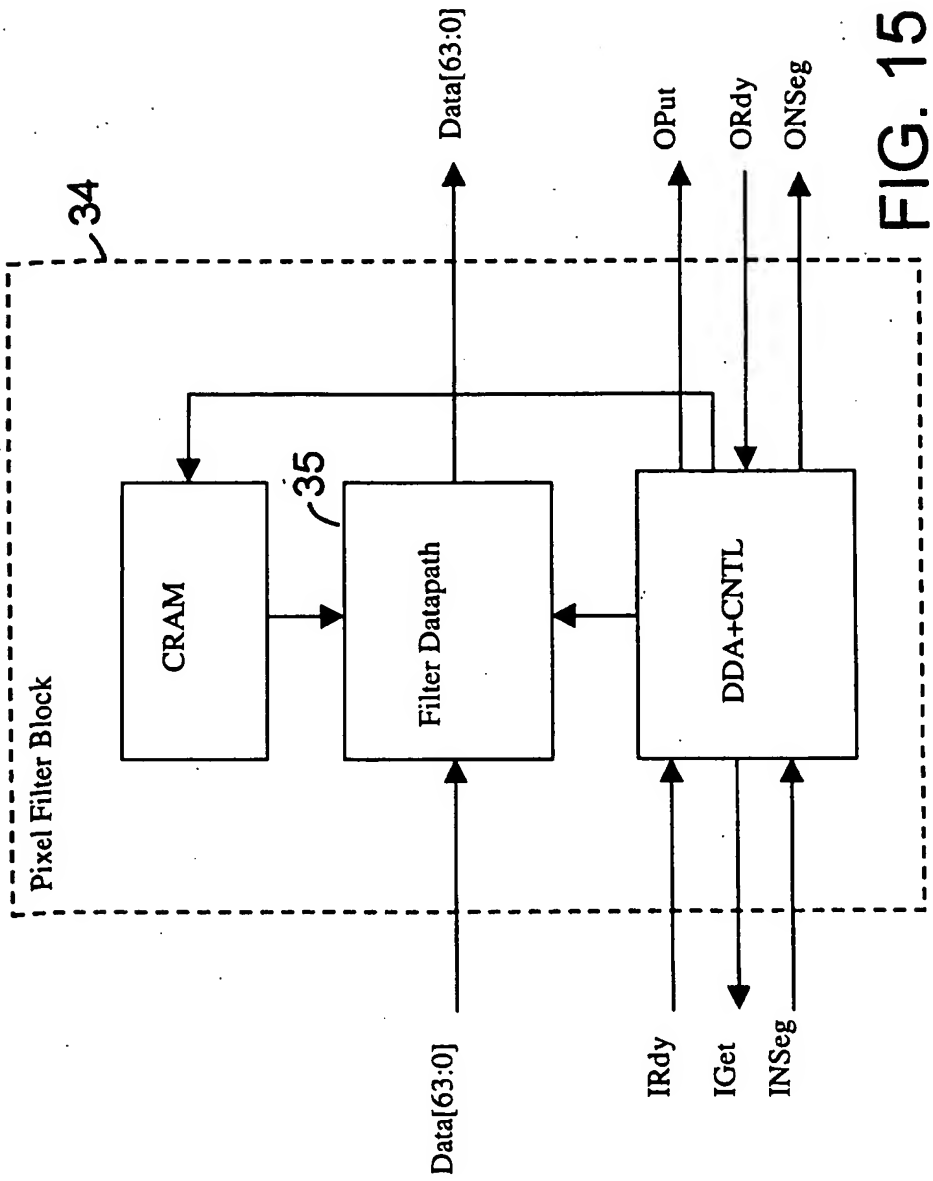

Data[63:0]
OPut
ORdy
ONSeg
34
35
CRAM
Filter Datapath
DDA+CNTL
Pixel Filter Block
Data[63:0]
IRdy
IGet
INSeg

FIG. 15

**Input Table**

| | Signal | Description |
|---|---|---|
| | | **Clock and Reset Interface** |
| | HVS_Reset | Hardware Vertical Scaler reset |
| | HVS_Clk | Hardware Vertical Scaler main clock |
| | | **Memory Interface** |
| 116 | Store_Ready | Memory Controller can accept output image data |
| | | **Register and Command Interface** |
| 106 | Y_Addr[31:3] | Upper 29 bits of the scaled Y image destination byte address |
| 108 | Y_Pitch[14:3] | Amount to add to the address to locate the next line's Y pixels |
| 110 | Y_Length[10:0] | Number of lines in the scaled output Y image plane |
| 112 | Y_Width[11:0] | Number of Y pixels (x4) in one line of the scaled image |
| 106 | U_Addr[31:3] | Upper 29 bits of the scaled U image destination byte address |
| 108 | U_Pitch[14:3] | Amount to add to the address to locate the next line's U pixels |
| 110 | U_Length[10:0] | Number of lines in the scaled input U image plane |
| 112 | U_Width[11:0] | Number of U pixels (x4) in one line of the scaled image |
| 106 | V_Addr[31:3] | Upper 29 bits of the scaled V image destination byte address |
| 108 | V_Pitch[14:3] | Amount to add to the address to locate the next line's V pixels |
| 110 | V_Length[10:0] | Number of lines in the scaled input V image plane |
| 112 | V_Width[11:0] | Number of V pixels (x4) in one line of the scaled image |
| | | **Filter Interface** |
| 100 | Store_Y | The Pixel Filter Block is processing the Y plane of pixels |
| 102 | Store_U | The Pixel Filter Block is processing the U plane of pixels |
| 104 | Store_V | The Pixel Filter Block is processing the V plane of pixels |
| 114 | Scaled_Data[31:0] | Scaled output image data from Pixel Filter Block |
| 114 | Scaled_Req | Request to transfer data from PFB to OPFB |

FIG. 16

**Output Table**

| | Signal | Description |
|---|---|---|
| | | **Memory Interface** |
| 116 | Store_Req | Request to the memory interface for the output image data |
| 116 | Store_Data[31:0] | Scaled output image data |
| 116 | Store_Addr[31:3] | Upper 29 bits of the scaled image current byte address |
| | | **Filter Interface** |
| 114 | Scaled_Ready | OPFB is ready to accept pixels from the PFB |

FIG. 17

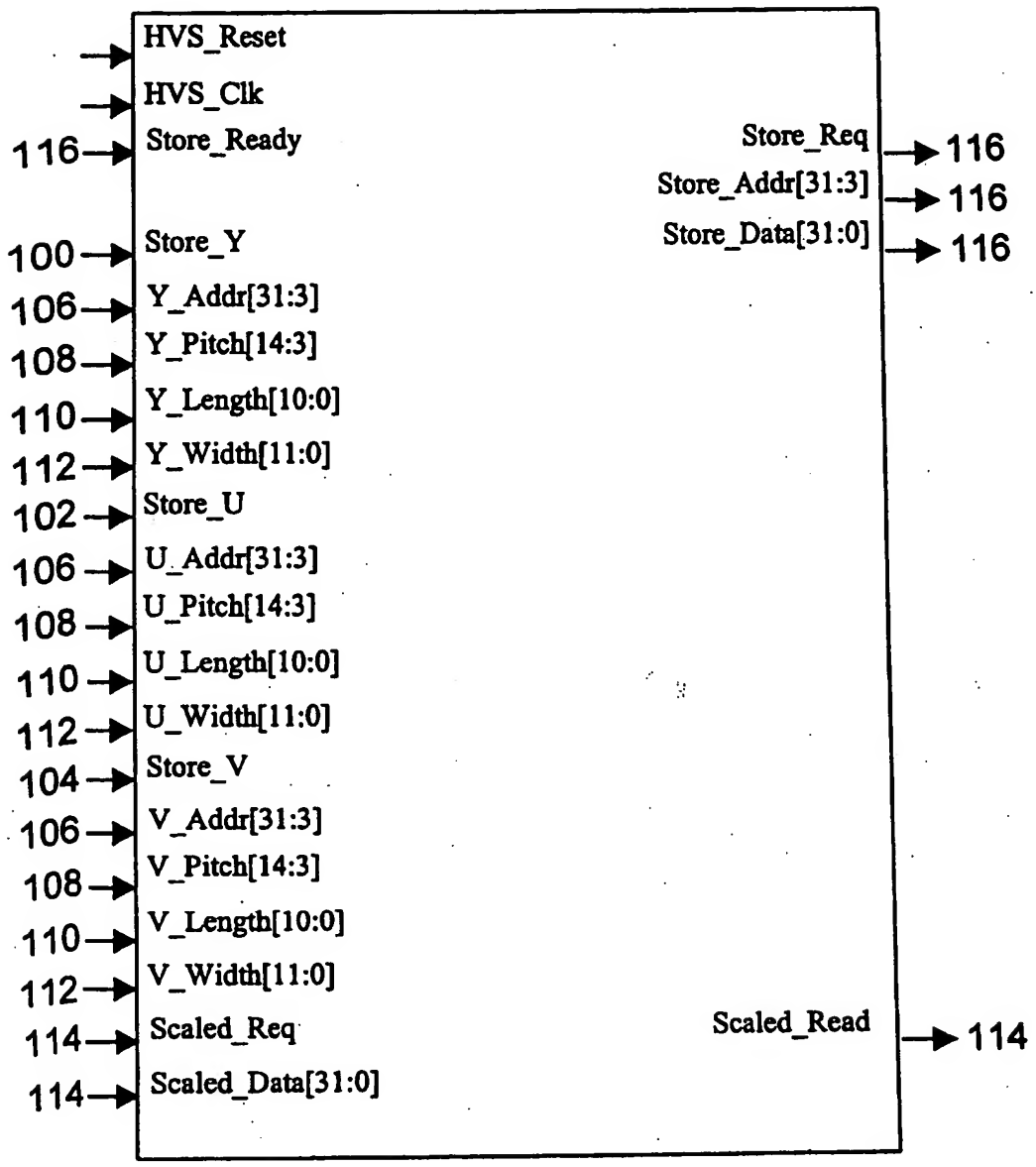

HVS_Reset
HVS_Clk
116
Store_Ready
Store_Req
116
Store_Addr[31:3]
116
Store_Data[31:0]
116
100
Store_Y
106
Y_Addr[31:3]
108
Y_Pitch[14:3]
110
Y_Length[10:0]
112
Y_Width[11:0]
102
Store_U
106
U_Addr[31:3]
108
U_Pitch[14:3]
110
U_Length[10:0]
112
U_Width[11:0]
104
Store_V
106
V_Addr[31:3]
108
V_Pitch[14:3]
110
V_Length[10:0]
112
V_Width[11:0]
114
Scaled_Req
Scaled_Read
114
114
Scaled_Data[31:0]

FIG. 18

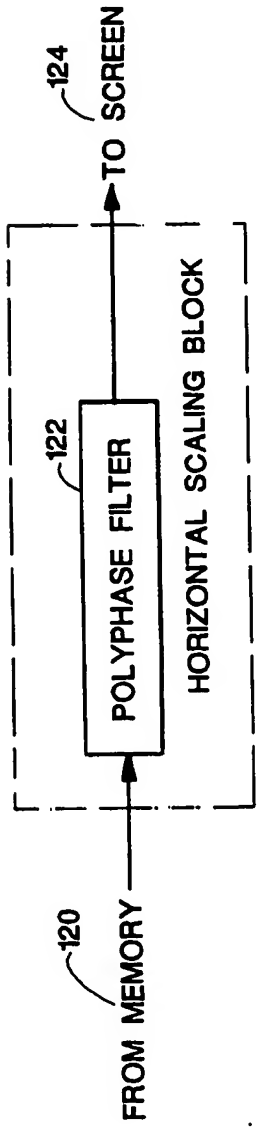

124
TO SCREEN
122
POLYPHASE FILTER
HORIZONTAL SCALING BLOCK
120
FROM MEMORY

FIG. 19